High Efficiency 7A Synchronous Boost Convertor

General Description

The LP6253 is a synchronous current mode boost DC-DC converter. Its PWM circuitry with built-in 7A(ESOP8) current power MOSFET makes this converter highly efficient. Selectable high switching frequency allows faster loop response and easy filtering with a low noise output. The non-inverting input its error amplifier is connected to an internal 0.5V(TQFN-16)/0.8V(ESOP8) precision reference voltage. Current mode control and internal compensation network make it easy and flexible to stabilize the system.

Features

- Up to 96% efficiency
- Output to Input Disconnect at Shutdown Mode
- Shut-down current:<1uA
- Output voltage Up to 5.0V/3A(ESOP8)
- Internal Compensation
- 1.4MHz(TQFN-16) & 800KHz(ESOP8)fixed frequency switching
- High switch on current:7A for LP6253SPF
  6A for LP6253QVF
- Available in ESOP8 and TQFN-16 Package

Applications

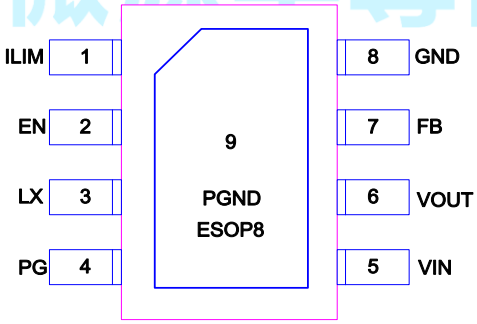
- Battery products
- Host Products
- Panel

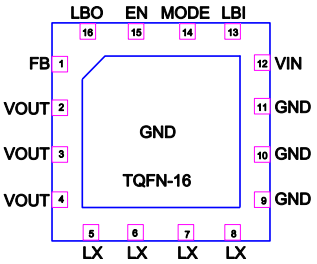
Ordering Information

LP6253 □ □ □

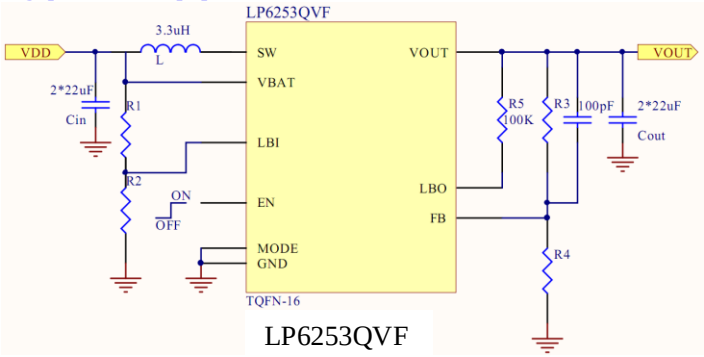
- F: Pb-Free
- Package Type
  - SP: ESOP8
  - QV: TQFN-16

Pin Configurations





Typical Application Circuit



LP6253QVF

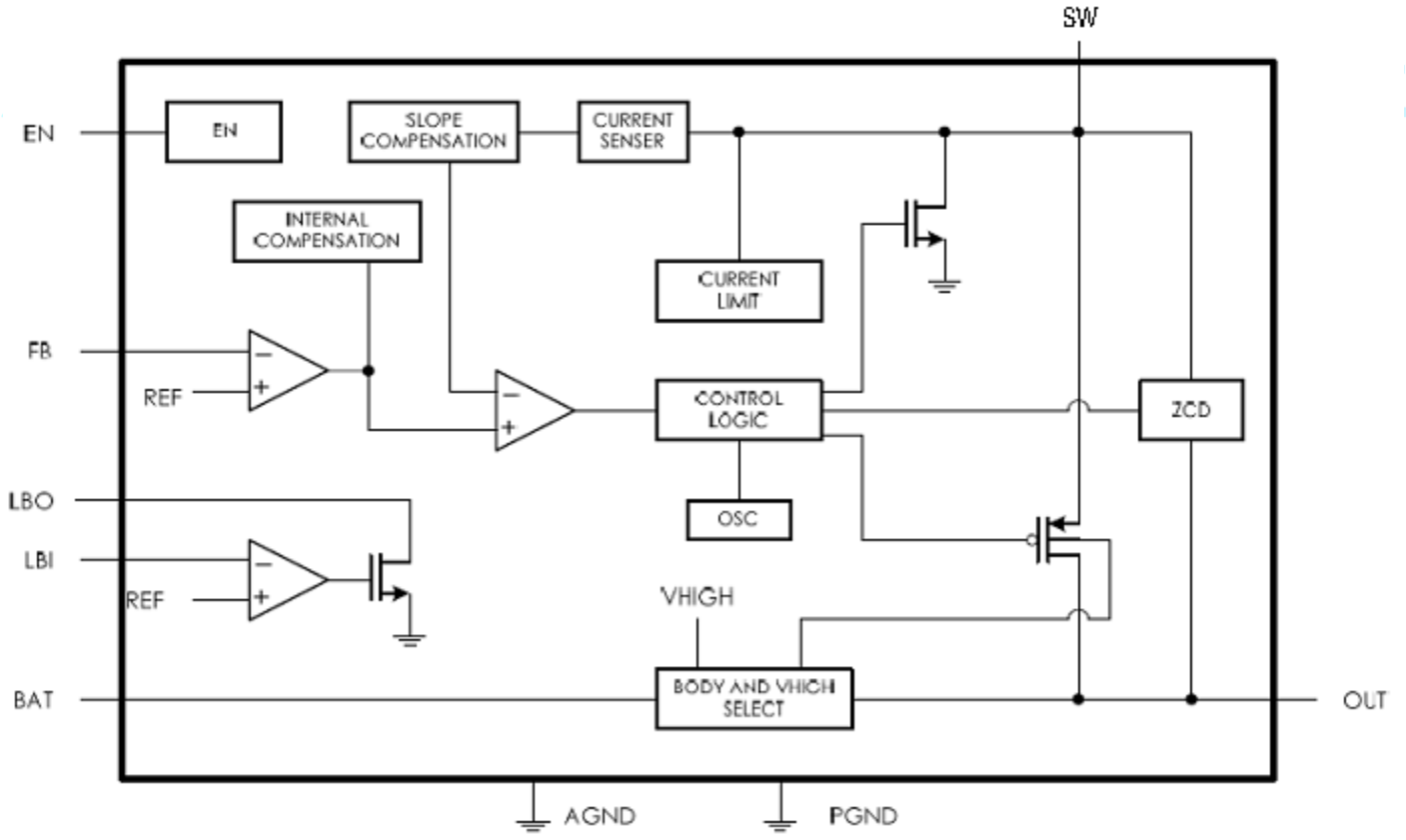
Marking Information

Device	Marking	Package	Shipping
LP6253SPF LP6253QVF	LPS LP6253 YWX	ESOP8 TQFN-16	3K/REEL
Y: Year code. W: Week code. X: Batch numbers.			

Functional Pin Description

ESOP8	TQFN-16	PIN Name	Description
7	1	FB	Feedback pin.
6	2,3,4	VOUT	Output pin.
3	5,6,7,8	LX	Switching pin.
8,9	9,10,11	GND	Ground pin.
5	12	VIN	Voltage input pin.
	13	LBI	Battery detector input pin.
	14	MODE	Enable power save mode. Low voltage active.
2	15	EN	Chip enable pin.
	16	LBO	Open_drain low battery detector output pin.
4		PG	Indication of power good. It is high resistance when VIN=0V, and connecting to ground when VIN>3V.
1		ILIM	By connection a resistor to ground, set the input current limit.

Function Block Diagram(for LP6253QVF)



Absolute Maximum Ratings

Supply Input Voltage ---------- 7V

Power Dissipation, P_D @ T_A = 25°C

ESOP8 ---------- 1.5W

TQFN-16 ---------- 1.5W

Package Thermal Resistance

ESOP8, θ_{JA} ---------- 46°C/W

TQFN-16, θ_{JA} ---------- 45°C/W

Lead Temperature (Soldering, 10 sec.) ---------- 260°C

Recommended Operating Conditions

Supply Input Voltage ---------- 2.6V to 5.5V

EN Input Voltage ---------- -0.3V to VIN+0.3V

Operation Junction Temperature Range ---------- −40°C to 125°C

Operation Ambient Temperature Range ---------- −40°C to 85°C

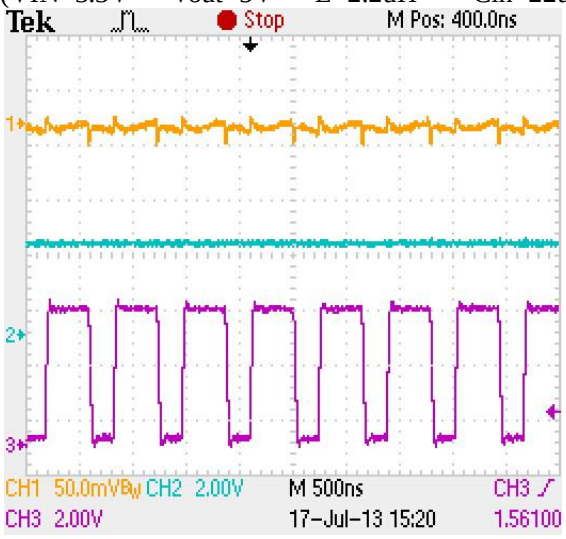
Electrical Characteristics

(Vin=3.5V,Vout=5V,Cin=22uF,Cout=22uF,L=2.2uH)

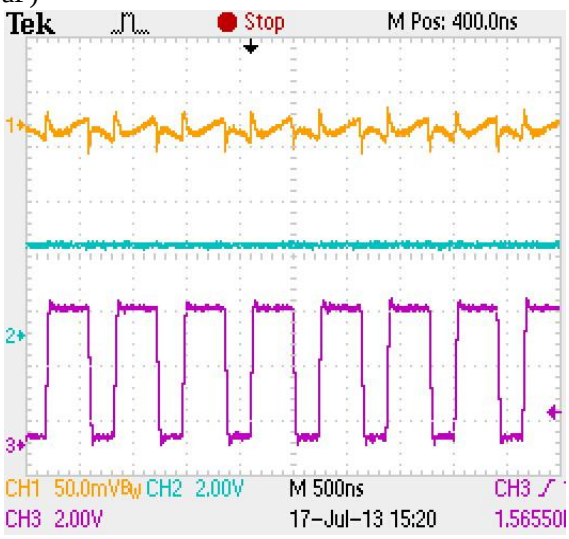
Parameter	Conditions	LP6253			Units
		Min	Typ	Max	
Supply Voltage		2.6		5.5	V
Output Voltage Range		2.6		5.5	V
Under voltage lockout	LP6253QVF, Vin voltage decreasing.		1.5		V
	LP6253SPF, Vin voltage decreasing.		2.3		
Supply Current(Shutdown)	VEN= 0V		0.05	1	uA
Supply Current	LP6253QVF,VFB=0.6V		190		uA
Feedback Voltage	LP6253QVF	0.49	0.5	0.51	V
	LP6253SPF	0.784	0.8	0.816	
Feedback Input Current	VFB=0.6V for LP6253QVF		50		nA
Switching Frequency	LP6253QVF	1200	1400	1600	KHz
	LP6253SPF	600	800	1000	
EN Input Low Voltage				0.4	V
EN Input High Voltage		1.4			V
Power mosfet Current Limit	LP6253SPF		7		A
	LP6253QVF		6		A
High-side On Resistance	Vout=5V		55		mΩ
Low-side On Resistance	Vout=5V		55		mΩ
Line regulation				0.6	%
LBI voltage threshold	LP6253QVF, VLBI voltage decreasing	490	500	510	mV
LBI input hysteresis	LP6253QVF,		10		mV
LBI input current	LP6253QVF, EN = VBAT or GND		0.01	0.1	uA
LBO output low voltage	LP6253QVF, VO=3.3V		0.04	0.4	V
LBO output low current	LP6253QVF,		100		uA
LBO leakage current	LP6253QVF, VLBO = 7 V		0.01	0.1	uA
Over temperature protection			150		°C
Over temperature hysteresis			20		°C

Typical Operating Characteristics(for LP6253QVF)

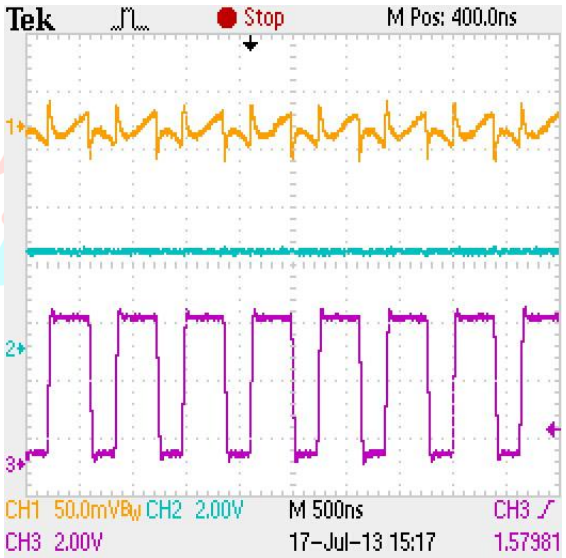
(VIN=3.3V Vout=5V L=2.2uH Cin=22uF Cout=22uF)



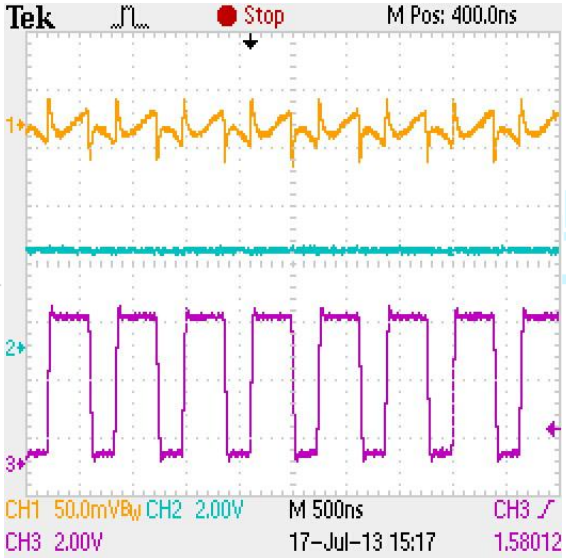
CH1=Vout, CH2=Vin, CH3=SW
ILOAD =500mA



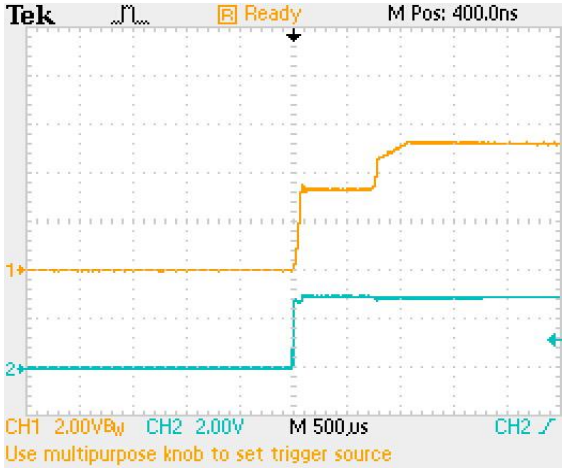
CH1=Vout, CH2=Vin, CH3=SW
ILOAD =1000mA



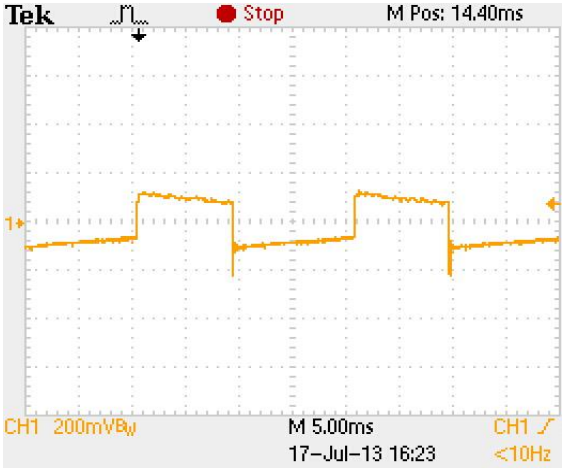
CH1=Vout, CH2=Vin, CH3=SW
ILOAD =2000mA



CH1=Vout, CH2=Vin, CH3=SW
ILOAD =2500mA

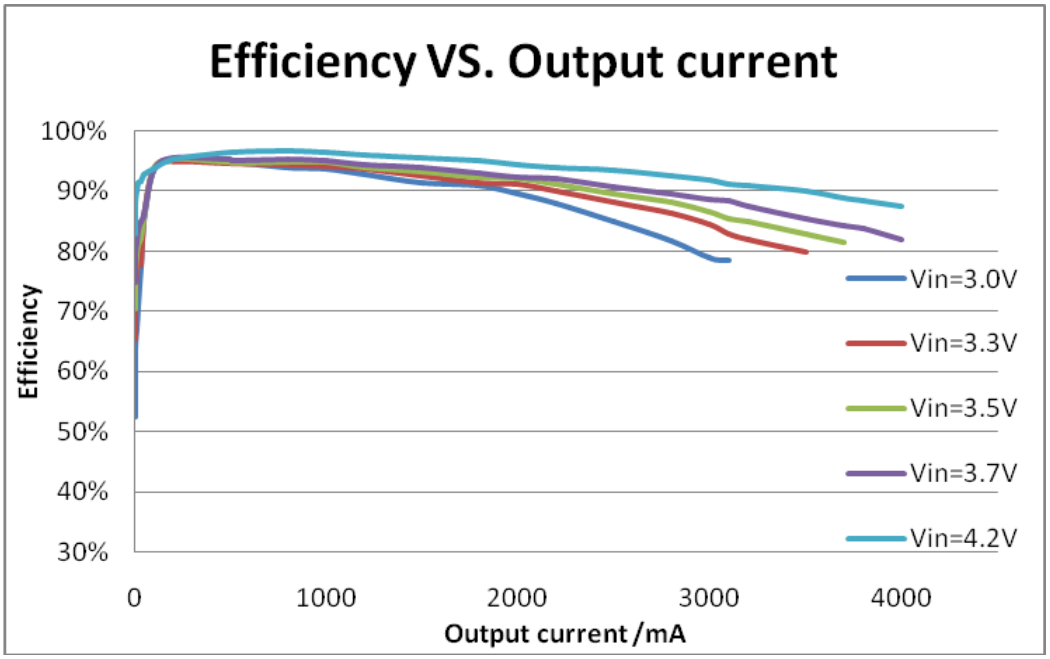


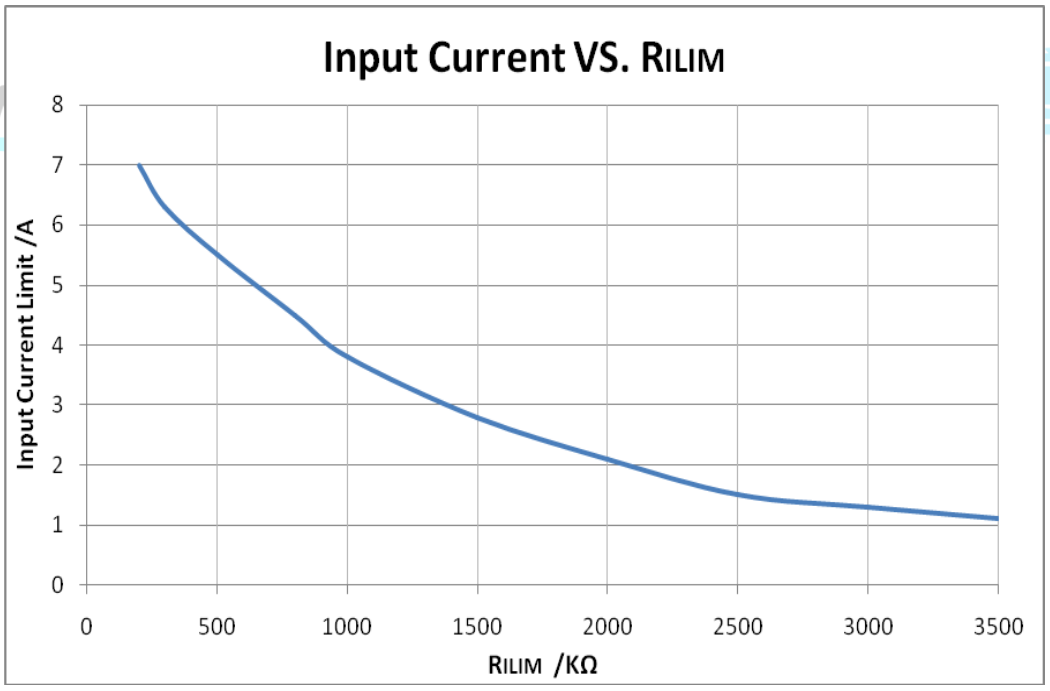
CH1=Vout, CH2=EN, ILOAD= 10mA



Vin=3.3V, Vout=5V, ILOAD=10mA—200mA

Typical Operating Characteristics(for LP6253SPF)





Operation Information

The LP6253 uses a synchronous 1.4MHz/800KHz fixed frequency, current-mode regulation architecture to regulate the output voltage. The LP6253 measures the output voltage through an external resistive voltage divider and compares that to the internal 0.5V/0.8V reference to generate the error voltage to the inductor current to regulate the output voltage. The use of current-mode regulation improves transient response and control loop stability. The peak current of the NMOS switch is also sensed to limit the maximum current flowing through the switch and the inductor. The typical peak current limit is set to 7A(LP6253SPF). An internal temperature sensor prevents the device from getting overheated in case of excessive power dissipation.

The device integrates an N-channel and a P-channel MOSFET transistor to realize a synchronous rectifier. Because the commonly used discrete Schottky rectifier is replaced with a low $R_{DS(ON)}$ PMOS switch, the power conversion efficiency reaches 96%. To avoid ground shift due to the high currents in the NMOS switch, two separate ground pins are used. The reference for all control functions is the GND pin. The source of the NMOS switch is connected to PGND. Both grounds must be connected on the PCB at only one point close to the GND pin. A special circuit is applied to disconnect the load from the input during shutdown of the converter. In conventional synchronous rectifier circuits, the backgate diode of the high-side PMOS is forward biased in shutdown and allows current flowing from the battery to the output. This device however uses a special circuit which takes the cathode of the backgate diode of the high-side PMOS and disconnects it from the source when the regulator is not enabled (EN = low). The benefit of this feature for the system design engineer is that the battery is not depleted during shutdown of the converter. No additional components have to be added to the design to make sure that the battery is disconnected from the output of the converter.

Device Enable

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND. In shutdown mode, the regulator stops switching, all internal control circuitry including the low-battery comparator is switched off, and the load is isolated from the input (as described in the Synchronous Rectifier Section). This also means that the output voltage can drop below the input voltage during shutdown. During start-up of the converter, the duty cycle and the peak current are limited in order to avoid high peak currents drawn from the battery.

Undervoltage Lockout

An under voltage lockout function prevents device start-up if the supply voltage on VBAT is lower than approximately 1.5V(LP6253QVF) & 2.3V(LP6253SPF). When in operation and the battery is being discharged, the device automatically enters the shutdown mode if the voltage on VBAT drops below approximately 1.5 V. This undervoltage lockout function is implemented in order to prevent the malfunctioning of the converter.

Softstart(for LP6253QVF)

When the device enables the internal start-up cycle starts with the first step, the precharge phase. During precharge, the rectifying switch is turned on until the output capacitor is charged to a value close to the input voltage. The rectifying switch current is limited in that phase. This also limits the output current under short-circuit conditions at the output. After charging the output capacitor to the input voltage the device starts switching. Until the output voltage is reached, the boost switch current limit is set to 40% of its nominal value to avoid high peak currents at the battery during startup. When the output voltage is reached, the regulator takes control and the switch current limit is set back to 100%.

Power Save Mode(for LP6253QVF)

The MODE pin can be used to select different operation modes. To enable power save, MODE must be set low. Power save mode is used to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with one or several pulses and goes again into power save mode once the output voltage exceeds the set threshold voltage. This power save mode can be disabled by setting the MODE to VBAT.

Low Battery Detection ---- LBI/LBO(for LP6253QVF)

The LP6253 low-battery detector circuit is typically used to supervise the battery voltage and to generate an error flag when the battery voltage drops below a user-set threshold voltage. The function is active only when the device is enabled. When the device is disabled, the LBO pin is high-impedance. The switching threshold is 500 mV at LBI. During normal operation, LBO stays at high impedance when the voltage, applied at LBI, is above the threshold. It is active low when the voltage at LBI goes below 500 mV.

The battery voltage, at which the detection circuit switches, can be programmed with a resistive divider connected to the LBI pin. The resistive divider scales down the battery voltage to a voltage level of 500 mV, which is then compared to the LBI threshold voltage. The LBI pin has a built-in hysteresis of 10mV, If the low-battery detection circuit is not used, the LBI pin should be connected to GND (or to VBAT) and the LBO pin can be left unconnected. Do not let the LBI pin float.

The recommended value for R2 is therefore in the range of 500kΩ. From that, the value of resistor R1, depending on the desired minimum battery voltage VBAT, can be calculated using:

LP6253QVF:R1=(VBAT/0.5V-1)×R2

Setting the Output Voltage

Set the output voltage by selecting the resistive voltage divider ratio. The voltage divider drops the output voltage to the 0.5V(LP6253QVF)/ 0.8V(LP6253SPF) feedback voltage. Use a 10K resistor for R4 of the voltage divider. Determine the high-side resistor R3 by the equation:

$$Vout=(R3/R4+1)\times V_{FB}$$

Low-EMI Switch

The device integrates a circuit that removes the ringing that typically appears on the SW node when the converter enters discontinuous current mode. In this case, the current through the inductor ramps to zero and the rectifying PMOS switch is turned off to prevent a reverse current flowing from the output capacitors back to the battery. Due to the remaining energy that is stored in parasitic components of the semiconductor and the inductor, a ringing on the SW pin is induced. The integrated antiringing switch clamps this voltage to VBAT and therefore dampens ringing.

Pre-Boost Current and Short Circuit Protect

Initially output voltage is lower than battery voltage, and the LP6253 enters pre-boost phase. During pre-boost phase, the internal NMOSFET/PMOSFET is turned off/on and a constant current is provided from battery to output until the output voltage close to the battery voltage. The constant current is limited by internal controller. If the output short to ground, the LP6253 also limits the output current to avoid damage condition.

Inductor Selection

For a better efficiency in high switching frequency converter, the inductor selection has to use a proper core material such as ferrite core to reduce the core loss and choose low ESR wire to reduce copper loss. The most important point is to prevent the core saturated when handling the maximum peak current. Using a shielded inductor can minimize radiated noise in sensitive applications. The maximum peak inductor current is the maximum input current plus the half of inductor ripple current. The calculated peak current has to be smaller than the current limitation in the electrical characteristics. A typical setting of the inductor ripple current is 20% to 40% of the maximum input current. If the selection is 40%, the maximum peak inductor current is

$$I_{PEAK} = I_{IN(MAX)} + \frac{1}{2} I_{RIPPLE} = 1.2 \times I_{IN(MAX)}$$
$$= 1.2 \times \left[\frac{I_{OUT(MAX)} \times V_{OUT}}{\eta \times V_{IN(MIN)}} \right]$$

The minimum inductance value is derived from the following equation :

$$L = \frac{\eta \times V_{IN(MIN)}^2 \times [V_{OUT} - V_{IN(MIN)}]}{0.4 \times I_{OUT(MAX)} \times V_{OUT}^2 \times f_{OSC}}$$

Depending on the application, the recommended inductor value is between 2.2μH to 10μH.

Input Capacitor Selection

For better input bypassing, low-ESR ceramic capacitors are recommended for performance. A 10μF input capacitor is sufficient for most applications. A ceramic capacitor or a tantalum capacitor with a 100nF ceramic capacitor in parallel,

placed close to the IC, is recommended .For a lower output power requirement application, this value can be decreased.

Output Capacitor Selection

For lower output voltage ripple, low-ESR ceramic capacitors are recommended. The tantalum capacitors can be used as well, but the ESR is bigger than ceramic capacitor. The output voltage ripple consists of two components: one is the pulsating output ripple current flows through the ESR, and the other is the capacitive ripple caused by charging and discharging. The major parameter necessary to define the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero, by using Equation:

$$V_{RIPPLE} = V_{RIPPLE\_ESR} + V_{RIPPLE\_C}$$

$$\cong I_{PEAK} \times R_{ESR} + \frac{I_{PEAK}}{C_{OUT}} \left(\frac{V_{OUT} - V_{IN}}{V_{OUT} \times f_{OSC}} \right)$$

Layout Guideline

For high frequency switching power supplies, the PCB layout is important step in system application design. In order to let IC achieve good regulation, high efficiency and stability, it is strongly recommended the power components should be placed as close as possible. The set races should be wide and short. The feedback pin and then works of feedback and compensation should keep away from the power loops, and be shielded with a ground trace or plane to prevent noise coupling.

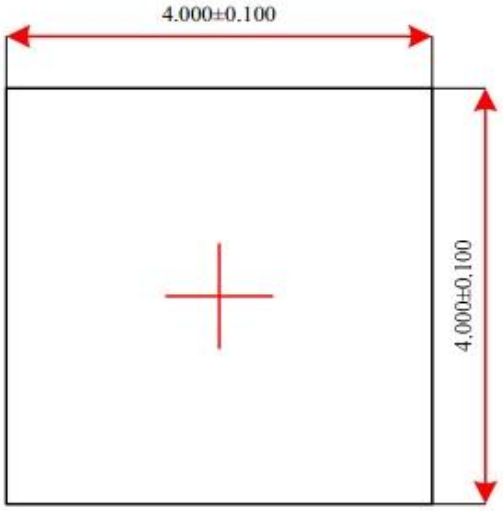
Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component. Three basic approaches for enhancing thermal performance are listed below:

Improving the power dissipation capability of the PCB design;

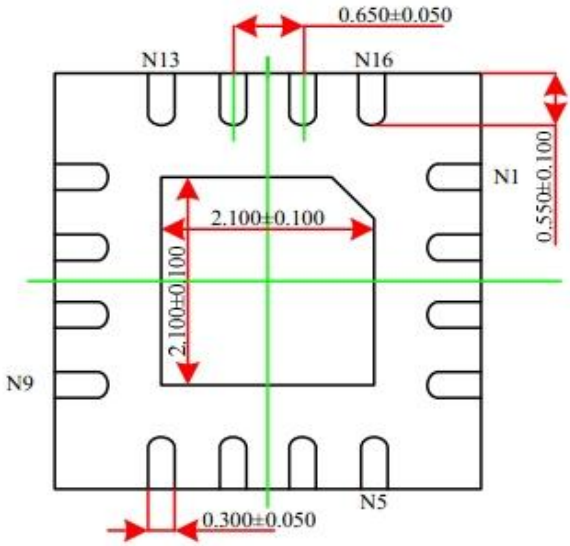
Improving the thermal coupling of the component to the PCB;

Introducing airflow in the system.

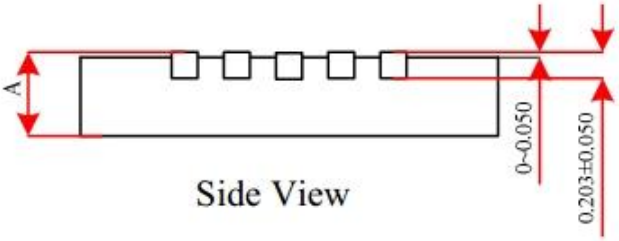
Packaging Information



Top View



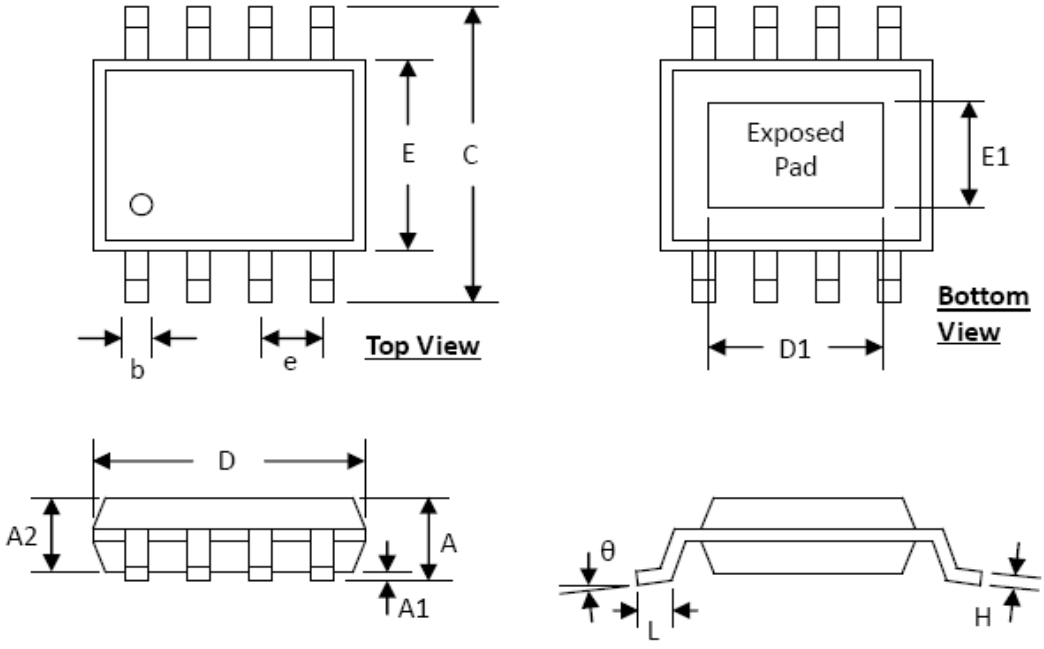
Bottom View



Side View

	MIN.	NORM.	MAX.
A	0.700	0.750	0.800
	0.800	0.850	0.900

ESOP8



SYMBOLS	DIMENSION (MM)		DIMENSION (INCH)	
	MIN	MAX	MIN	MAX
A	1.30	1.70	0.051	0.067
A1	0.00	0.15	0.000	0.006
A2	1.25	1.52	0.049	0.060
b	0.33	0.51	0.013	0.020
C	5.80	6.20	0.228	0.244
D	4.80	5.00	0.189	0.197
D1	3.15	3.45	0.124	0.136
E	3.80	4.00	0.150	0.157
E1	2.26	2.56	0.089	0.101
e	1.27 BSC		0.050 BSC	
H	0.19	0.25	0.0075	0.0098
L	0.41	1.27	0.016	0.050
θ	0°	8°	0°	8°